cancellation filter 14 according to the invention has a constant input resistance on account of the amplifier input stage.

The echo cancellation filter 14 according to the invention which is illustrated in figure 3 requires only one active amplification stage and therefore has only a very small number of active circuit components. Therefore, the power consumption of the echo cancellation filter 14 according to the invention is very low and, what is more, the noise power of the echo cancellation filter 14 according to the invention is very low. In a preferred embodiment, the operational amplifier 39 of the echo cancellation circuit 14 is supplied with a low supply voltage of just 3.3 V via the supply voltage terminals 40a, 40b. In a preferred embodiment, the noise of the echo cancellation filter 14 preferably lies below -148 dBm/Hz, the power consumption being only 25 mW in the case of a frequency band of 1.1 MHz. The TDH (Total Harmonic Distortion) is less than -85 dB.

The area requirement of the echo cancellation filter 14 according to the invention, as illustrated in figure 3, is just 0.33 mm^2, e.g. in the case of a 0.65 µ fabrication process, and is thus very small.

The transfer function of the echo cancellation filter 14 according to the invention is adjustable in a simple manner by the DSP processor 21. The echo cancellation filter 14 is preferably a first-order low-pass filter. In this case, the gain of the echo cancellation filter is separately adjustable by the DSP processor in a frequency range lying below a first cut-off frequency and in a frequency range lying above a second cut-off frequency. In this case, the two cut-off frequencies of the echo cancellation filter are likewise adjustable by the DSP processor 21.

Figure 5 shows the frequency response of a preferred embodiment of the echo cancellation filter 14 according to the invention. The adjustable gain of the echo cancellation filter amounts to H_1 up to a lower cut-off frequency f_U and the adjustable gain of the echo cancellation filter 14 amounts to H_2 above an upper cut-off frequency f_O. In the transition frequency range between the lower cut-off frequency f_U and the upper cut-off frequency f_O, the gain decreases e.g. by 20 dB per decade. The DSP processor 21 can adjust the gain H_1 of the echo cancellation filter 14 and also the two cut-off frequencies f_U, f_O by driving the controllable switches 66 contained in the resistor circuits.

The transfer function of the echo cancellation filter 14 illustrated in figure 3 reads as follows:

$$H(w) = K \cdot \frac{1 + jwC_{58}\dfrac{R_{43} \cdot R_{51}}{R_{55} + R_{43} + R_{51}}}{1 + jwC_{58}\dfrac{R_{43} \cdot R_{51}}{R_{43} + R_{51}}} \qquad (1)$$

where the gain k is:

$$K = \frac{R_{48}}{R_{36}} \cdot \frac{R_{25}}{R_{55}} \left(1 + \frac{R_{55}}{R_{43} + R_{51}}\right) \qquad (2)$$

The resistances R_{48}, R_{51}, R_{55} of the three programmable resistor circuits 48, 51, 55 are adjustable or programmable by the DSP processor 21 for setting the gain, the upper cut-off frequency f_O and the lower cut-off frequency f_U.

The resistances R_{36} and R_{43} of the input resistors 36 and of the output resistors 43 are constant, just like the resistance R_{25} of the input resistor of the

automatic gain control circuit. The capacitance C_{58} of the capacitor 58 is also fixedly prescribed.

Through the programming or setting of the resistor circuits 48, 51, 55, the DSP controller 21 is able to alter the frequency response of the echo cancellation filter 14, as is illustrated in figure 5, in accordance with the transmitted transmission signal and the changes in impedance that occur on the signal line. On account of the minimal voltage swings at the controllable switches 66 contained in the programmable resistor circuits 48, 51, 55, the linear signal distortions that occur become minimal in this case, with the result that the echo cancellation signal 14 completely cancels the echo signal that occurs. The echo cancellation filter 14 according to the invention requires only one capacitor 58, which, moreover, can be mounted externally using SMD technology in an area-saving manner. The echo cancellation circuit 14 according to the invention contains only one active amplifier stage 39 for impedance decoupling, with the result that the power consumption of the echo cancellation filter 14 according to the invention is low and the echo cancellation filter 14 itself has a very low noise power. The algorithm required for programming the echo cancellation filter 14 within the DSP processor 21 is relatively simple, with the result that the circuitry outlay for the DSP processor 21 likewise decreases.

The echo cancellation filter 14 according to the invention is particularly suitable for incorporation in transceivers for xDSL signals.